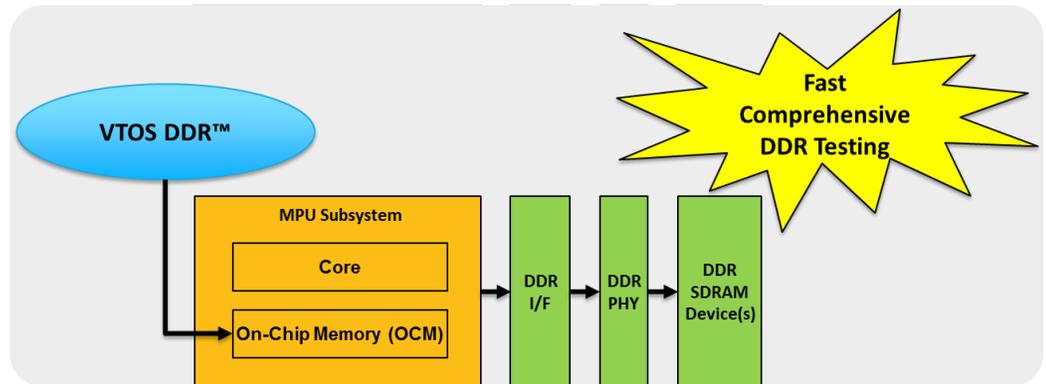


# VTOS DDR™

## Everything you need to configure, verify and tune DDR

During printed circuit board test, a valuable first step is to prove that all DDR memory is functioning properly. Properly operating DDR memory is a key requirement for properly executing software.

VTOS DDR is a low-cost software product that provides everything you need to configure, verify, and tune the DDR memory of your board design.



VTOS DDR is a standalone DDR verification tool that integrates with JTAG hardware and with Kozio's vAccess™ for automated production test. In standalone mode, VTOS DDR is loaded into on-chip memory and provides a dedicated user interface. When integrated with vAccess, you can use NI's TestStand, a custom test executive, or supported third-party user interfaces.

Kozio's VTOS DDR provides a fast and comprehensive software solution for configuring and functionally testing all of DDR memory. VTOS DDR is a bare-metal application that executes from an MPU's on-chip memory and requires no other software, operating system, or boot loader – making VTOS DDR an excellent solution for new circuit board designs.

## Verifying DDR Memory

VTOS DDR is a small executable that runs directly from on-chip memory, allowing you to fully test DDR memory before any software executes from it. It allows you to specify your own DDR settings, based on example DDR settings from Kozio.

VTOS DDR provides a rich and comprehensive set of memory tests:

- Walking 0's and 1's Test
- Address Line Test
- Data Bus Noise Test
- Memory Cell Test
- March Address Test
- Data Bus Noise Test
- Burst Transfer Test
- Simultaneous Switching Output Test
- Performance Tests

VTOS DDR is loaded into on-chip memory using JTAG and a simple JTAG configuration script. VTOS DDR establishes a communications link with software running on a PC, utilizing the same JTAG interface, or a UART connection. Once executing, delivered scripts are used for on-the-fly DDR configuration, testing, and tuning.

The screenshot shows the VTOS DDR software interface. On the left is a 'Configuration' tree with various test categories like 'Board Initialization', 'Scripts', and 'SOC'. Under 'SOC', there are 'DDR Settings' and 'DDR Comprehensive Test' (which is highlighted). On the right is a 'Config Mode' / 'Run Mode' terminal window showing the following test results:

```

Addr configure
Configuring DDR3 memory controller
Creating local access window for DDR3
Enabling the DDR3 controller
DRAM configuration is complete
Memory configuration complete: memory size = 512 MiB

test.adram.walk0 // DDR Walking 0 Test
SDRAM: Walking 0 (32-bit) [00000000_00000000]
[PASSED]

test.adram.walk1 // DDR Walking 1 Test
SDRAM: Walking 1 (32-bit) [00000000_00000000]
[PASSED]

test.adram.address // DDR Address Test
SDRAM: Address bus [00000000_00000000 - 00000000_ffffff]
[PASSED]

test.ddr.structural // DDR Structural Test
SDRAM Memory Structural Suite:SDRAM: Walking 0 (32-bit) [00000000_00000000]
SDRAM: Walking 1 (32-bit) [00000000_00000000]
SDRAM: Address bus [00000000_00000000 - 00000000_ffffff]
Test Suite Totals: 3 Passed, 0 Failed, 0 Aborted, Running time 0.369 secs
[PASSED]

test.ddr.noise // DDR Noise Group Test
SDRAM Memory Noise Suite:SDRAM: Simult switch (32-bit) [00000000_00000000 - 00000000_ffffff]
SDRAM: Memory bus noise [00000000_00000000]
SDRAM: Memory bus noise (burst) [00000000_00000000 - 00000000_ffffff]
Test Suite Totals: 3 Passed, 0 Failed, 0 Aborted, Running time 2.973 secs
[PASSED]

test.ddr.comprehensive // DDR Comprehensive Test
SDRAM Memory Comprehensive Test Suite:SDRAM: Walking 0 (32-bit) [00000000_00000000]
SDRAM: Walking 1 (32-bit) [00000000_00000000]
SDRAM: Address bus [00000000_00000000 - 00000000_ffffff]
SDRAM: Simult switch (32-bit) [00000000_00000000 - 00000000_ffffff]
SDRAM: Memory bus noise [00000000_00000000]
SDRAM: Full (8 bit) [00000000_00000000 - 00000000_ffffff]
SDRAM: Full (32 bit) [00000000_00000000 - 00000000_ffffff]
SDRAM: Full burst (32 bit) [00000000_00000000 - 00000000_ffffff]
SDRAM: Memory bus noise (burst) [00000000_00000000 - 00000000_ffffff]
Test Suite Totals: 9 Passed, 0 Failed, 0 Aborted, Running time 8.841 secs
[PASSED]

```

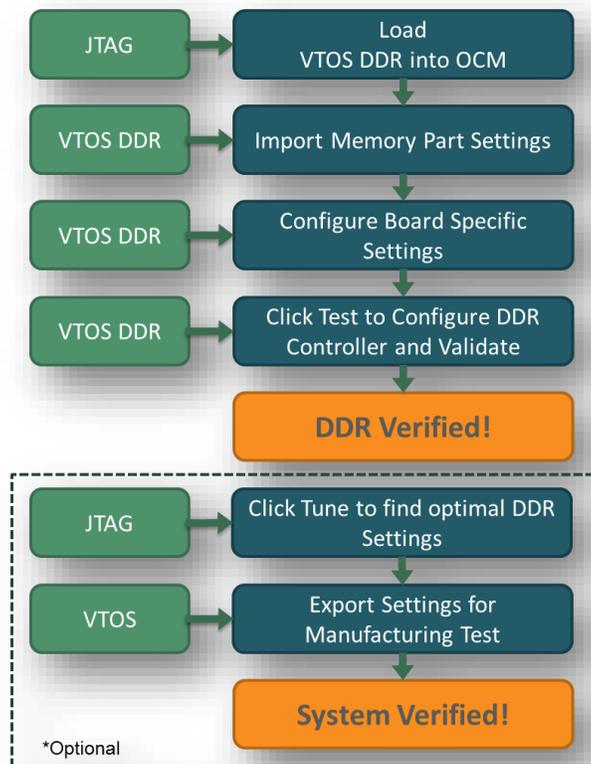
## VTOS DDR™ Provides

- A rich suite of directed memory tests that verify the entire 64-bit DDR memory range, including address testing, burst testing, noise testing, and stress testing.
- DDR configuration for DDR2, DDR3, DDR4, and mDDR (LPDDR) memory controllers.
- Constrained random capabilities for extended memory testing and burn-in.
- A powerful scripting environment for automated tuning of DDR settings.
- Highly optimized test algorithms that make it possible to test every cell of memory in production.
- Easy exporting for automated test.

## DDR Test Process Flow

Follow these steps to thoroughly verify your DDR memory:

- VTOS DRR is ready for use via a software downloads page. A license is required for full product activation.
- Using JTAG, load VTOS DDR executable into on-chip memory.
- Using the VTOS DDR GUI, load board specific settings and memory part information, verify and tune DDR memory.
- The total test time varies, but comprehensive DDR verification can be completed in seconds. Tuning usually takes under 30 minutes.
- With DDR configured and verified, export your test configuration for test automation.



## Design Benefits

- Slash DDR configuration/tuning efforts
- Stable debug interface for updating any DDR register
- Streamlined JTAG integration
- No code compiling & downloading
- Full support for mDDR, LPDDR, DDR2, DDR3, and DDR4 memories

## Production Benefits

- Comprehensive DDR verification
- Fast test times
- Easy integration with TestStand, LabVIEW, and other test executives
- Complete API for custom applications
- Easily fits into your manufacturing process

## Additional Product Information

VTOS DDR is available for designs utilizing TI's Sitara processors, Freescale's i.MX6, QorIQ, and PowerQUICC processors. Additional processor support is being added based on customer demand. VTOS DDR requires 32 KiB or more of on-chip memory. VTOS DDR can communicate with a PC over a JTAG or serial connection. Reduce your time and effort verifying new DDR settings, testing your prototypes and manufactured units, and debugging software issues knowing you have stable memory.

For additional information:

- Email [sales@kozio.com](mailto:sales@kozio.com)
- Or call +1 303-776-1356 x1