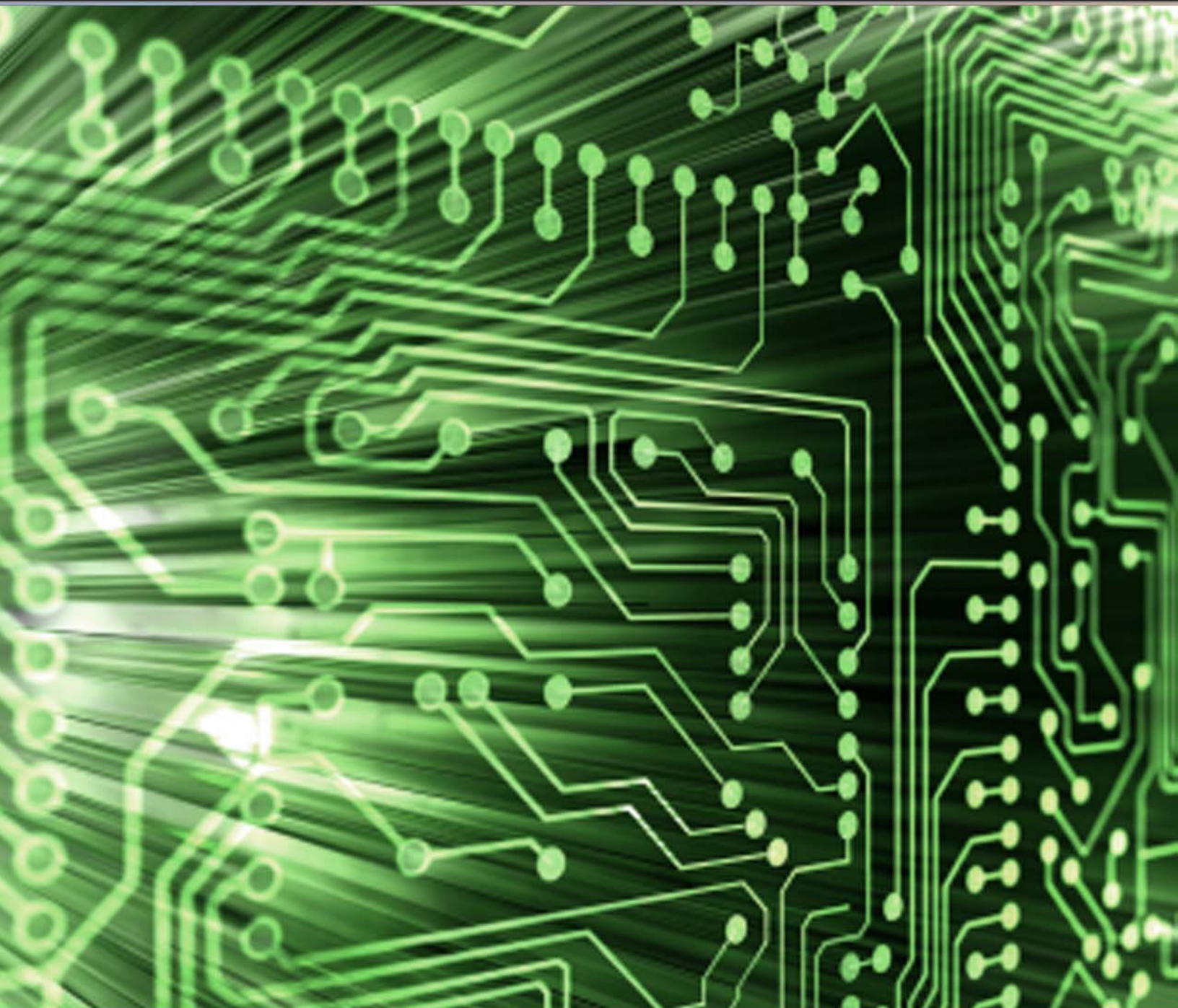


INSIDERS' GUIDE: EMBEDDED BOARDS & SYSTEMS



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KOZIO, INC.: EMBEDDED TEST SOLUTIONS

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Q. First of all, tell us a little bit about yourself and Kozio.

- A. I have been working for 20 years with embedded software and custom electronic devices for Kozio as well as military and storage companies. I am the co-inventor on 20 patents and I am co-founder of Kozio with Keith Short, based in Colorado. Best of all, I have an amazing wife and family.

Kozio provides software tools for automated circuit board testing and troubleshooting. The tools are valuable for testing hardware, troubleshooting design and assembly issues, automatic memory (DDR2) tuning and validation, self-test, as well as a software example for how to get the hardware working. Kozio is the first commercial provider of a comprehensive functional test solution. This type of test solution has typically been created in-house by the companies designing new circuit boards, much like OSs were years ago.

Q. Many of the vendors in this Guide concentrate on off-the-shelf, “standard” boards, whereas almost 45% of our user survey respondents indicate that they are doing a custom board. Can you briefly explain your software products and how they help with board test?

- A. We compliment JTAG emulated test and Boundary Scan testing by providing embedded at-speed functional testing of the circuit board. The key difference is that our software runs on the device and controls all aspects of how the hardware operates. Our overall package provides focus, flow, stress, and performance testing of a system-on-a-chip (SoC) and circuit board. Our solution validates entire data paths beyond the board and back, increasing the test coverage and providing a test solution that ships with the device.

For “standard” boards, we provide tools to the manufacturer. The end user may not ever see the test software. They use these tools for design verification as well as testing and serialization during volume production. Our products interactively test and troubleshoot a single device, or simultaneously test and track multiple boards. Our products save months of effort developing test code and getting the hardware running. For manufacturing test, they use a single button to launch an automated process to test, download images, program the device, and record all test results.

For “custom” boards, we provide very similar value, but this value is often increased because the customer may not have prior experience with a processor and may not have the staff or time to develop a comprehensive hardware test tool. Our expert team provides very efficient support in all aspects of determining if the hardware works as well as helping to get it to work. For example, many customers have spent several months trying to resolve DDR issues. Kozio tools and support determined root cause in days; presenting a clear path to correction and clear validation that DDR was working.

Q. High speed interconnects like PCI Express, RapidIO, and 10GE are all hotly competitive right now in the boards market. What insights can you share for board designers that are using one or more of these interconnects?

A. All three interconnects (PCI Express, RapidIO, 10GE) offer advantages and new challenges. Two important areas to cover in their design verification is concurrent stress testing and full data path verification. Full data path verification is also critical for production testing.

Functional test code is a great way to stress the interconnect (PCI Express, RapidIO, 10GE), buses, and memories. For stress testing, we recommend using multiple advance processor features, such as DMA transfers, caching and interrupts, to maximize the potential for timing and concurrency issues. Using stress testing can isolate issues related to processor and memory busses. In regards to DDR memory, advanced tuning and validation insures stable memory configurations.

Testing beyond the board's edge is also critical in isolation potential assembly errors. Testing an Ethernet connection at 10/100 speeds can pass while testing at 1GE and 10GE fail, because those interconnects use additional signals. PCI Express and RapidIO require additional test steps to test multiple data paths concurrently. We suggest testing across all interconnects, and board to board, to wring out and isolate issues with the higher speed interconnects.

Q. You mentioned in your emails before this interview the importance of "schematic review," especially by "software eyes." What are the unique values that having software perspective can bring to schematic review in board design?

A. Having a software team review schematics provides insight into what it will take to get the OS and application running on a circuit board design. This is true for both standard and custom boards. The more experience the software team has with numerous processors and board designs, the greater the feedback. I have seen over the years that a new electronic design requires 6-7 software engineers for every hardware engineer. The best aspect of a software review of a new hardware design is in keeping the cost of software development down.

A software review can provide feedback on whether an existing driver can be used or if a new driver has to be written. We have seen cases where a hardware design was outsourced to a design firm and their design, because they did not understand fully how the processor worked, resulted in additional driver development effort for the software team. A software review can also reduce the introduction of non-standard hardware features, such as an interface using 16-bits where the standard uses 8-bits. The software team can also provide feedback on which vendor to use, enabling software reuse.

Our firmware team reviews the schematics of most customers; we supported some military projects without the use of schematics. During schematic review, our team found issues that would have presented a component from working. For example, a PCI Express bus was missing a resistor.

Q. Memory is another area in which technology is quickly advancing; yet it becomes a design bottleneck for custom boards. How does your technology help with memory design challenges?

A. Our technology helps memory design challenges by providing automated configuration, tuning, and validation. We also provide a self-test product that is shipped with the circuit

board to test the memory on a regular basis. The quicker a design team can get to stable memory the faster the time to market.

We recently published a white paper titled “*A Comprehensive Memory Validation Strategy Using Advanced Processor Features*” which details insider tips and strategies for overcoming memory design issues.

Our expert team also provides valuable support based on prior experience with hundreds of unique circuit board designs. We can also offer the service of running our validation suite on a custom board, the customer just ships us the board and we provide a detailed analysis of test runs and results. We have seen companies struggle for months trying to get DDR memory working and get great results from us in days.

Q. And what about “design for manufacturability?” One of the big headaches in custom boards is the transition from prototype to production. What does Koizio do to make this transition easier?

- A. Koizio provides an integrated solution for one-button volume testing of circuit boards. We are the only commercial provider to deliver embedded test software integrated with powerful test management software. A test operator loads a pre-defined test sequence and selects run. The package supports one or more test stations and provides a very innovative solution for testing multiple devices simultaneously (in Beta now).

Creating a test sequence requires no programming. Our test sequences call test actions, and the designer simply chooses the test actions, and test cases, most appropriate for their process. Test actions make it easy to interface with the central database, call JTAG programmers, download images to the device under test, and automate a variety of board sequencing steps. Test scripts stored in the database can be used to test a various circuit board designs automatically.

The software tracks all test results in a central database and all products communicate over a local area network. A manager can create a custom report of all boards tested by one or more operators from his/her office or from the factory floor.

Q. Finally, share with us some of the business issues. What is a typical customer like for you? What would be the smallest custom board engagement that would be feasible for you?

- A. Koizio’s typical customer is a company using a circuit board design to produce an electronic device. We work directly with design engineers, test engineers, and engineering management, in the design and manufacturing sides of the business. Our typical engagement is that we receive hardware schematics and deliver embedded software configured for their board design in two weeks. Our customers are very happy with the return they get from purchasing our products.

A key qualification is that our *kDiagnostics*® product supports the processor they are using. We currently support 32-bit processors from AMCC, Freescale, IBM, and Intel. However, we are also continually adding support for new processors. For example, this month we are adding support for the Freescale Industrial processor family, the *MPC8554* and like. Our greatest business challenge right now is keeping up with the requests to support new processors.

Customers receive a development kit that allows them to use our diagnostics libraries to create custom test routines. Customers can choose to purchase *kDiagnostics* for their initial hardware testing and troubleshooting efforts, and then purchase our manufacturing suite later. This provides a low-cost entry into using our products. The

customer licenses the test management tools once and can use them to test multiple designs.

The customer realizes a return on investment with even the smallest custom board engagement. For design, we cost about $\frac{1}{4}$ the cost of doing themselves. For a customer manufacturing a low volume of boards, excluding savings during design verification, they begin saving money after testing 1,000 devices. This is only taking into account the technician time saved per board. We have one Tier 1 customer who is saving 3,000 test hours per year using our solution.

Q. How can custom board designers maximize test coverage?

- A. Most companies use a variety of test methods to create a combination that maximizes coverage and fault isolation, while keeping cost under control. However, all companies use some sort of software to test the assembled circuit board. In years past, the only choice was to use application software, or spend months or years coming up with a suitable test application. Using application software may seem like a viable test solution, but they rarely provide the fault coverage desired, and lack the features of deterministic execution and fault isolation.

A company may choose to create a suitable test application to insure the hardware is most reliable, but it may not be in their best business interest. In those cases, Koizio offers a new commercial solution for validating hardware using software. We offer several valuable advantages: test software is our focus, we support more board designs in 1 year than most companies see in 40, our test features grow exponentially, and we collaborate with the chip companies for an inside track on new technologies.

Q. Thank you for this interview.